

SN 10/620,179

Sheet 1 of 4

Form PTO-1449 INFORMATION DISCLOSURE CITATION IN AN APPLICATION <i>(Use several sheets if necessary)</i>		Docket Number (Optional) 3351.8US (96-0223.07/US) Applicant Brent Ke th Filing Date July 14, 2003		Application Number Not yet assigned Group Art Unit Unknown	
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U.S. PATENT DOCUMENTS						
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
UN	4,536,947	08/1985	Bohr et al.			
UN	4,742,018	05/1988	Kimura et al.			
UN	4,914,502	04/1990	Lebowitz et al.			
UN	4,922,460	05/1990	Furutani et al.			
UN	4,967,396	10/1990	Kajigaya et al.			
UN	4,970,564	11/1990	Kimura et al.			
UN	5,014,110	05/1991	Satoh			
UN	5,107,459	04/1992	Chu et al.			
UN	5,138,412	08/1992	Hieda et al.			
UN	5,170,243	12/1992	Dhong et al.			
UN	5,206,183	04/1993	Dennison			
UN	5,208,180	05/1993	Gonzalez			
UN	5,243,558	09/1993	Saeki			

FOREIGN PATENT DOCUMENTS							
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO
UN	3-174765	07/1991	Japan				
UN	60-258795	12/1984	Japan				
UN	4433695	03/1995	Germany				
UN	0078338	05/1983	EPO				

OTHER DOCUMENTS		(Including Author, Title, Date, Pertinent Pages, Etc.)
UN		Ahn et al., "Bidirectional Matched Global Bit Line Scheme for High Density DRAMS", (Abstract), pps. 91-92.
UN		Hamada et al., "A Split -Level Diagonal Bit-Line (SLDB) Stacked Capacitor Cell for 256MbDRAMs", IEEE, April, 1992, pps. 799-802.
UN		Inoue et al., "A 16Mb DRAM with An Open Bit-Line Architecture", International Solid State Circuits Conference, IEEE, 1988, pps. 246-247.

EXAMINER <i>V. Nguyen</i>	DATE CONSIDERED <i>4/5/04</i>
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance. Include copy of this form with next communication to the applicant.

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Sheet 2 of 4

Form PTO-1449 INFORMATION DISCLOSURE CITATION IN AN APPLICATION <i>(Use several sheets if necessary)</i>				Docket Number (Optional) 3351.8US (96-0223.07/US)		Application Number Not yet assigned	
				Applicant Brent Keeth		2818	
				Filing Date July 14, 2003		Group Art Unit Unknown	

U.S. PATENT DOCUMENTS						
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
W	5,280,443	01/1994	Hidaka et al.			
W	5,315,542	05/1994	Melzner			
W	5,396,450	03/1995	Takashima et al.			
W	5,396,451	03/1995	Ema			
W	5,499,205	03/1996	Ahn et al.			
W	5,534,732	07/1996	DeBrosse et al.			
W	5,581,126	12/1996	Moench			
W	5,625,234	04/1997	Suzuki et al.			
W	5,670,815	09/1997	Childs et al.			
W	5,680,347	10/1997	Takeuchi et al.			
W	5,815,428	09/1998	Tsuruda et al.			
W	5,838,038	11/1998	Takashima et al.			
W	5,864,181	01/1999	Keeth			
W	5,877,976	03/1999	Lattimore et al.			

FOREIGN PATENT DOCUMENTS							
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO

OTHER DOCUMENTS		(Including Author, Title, Date, Pertinent Pages, Etc.)
W		Kimura et al., "A Block-Oriented RAM with Half-Sized DRAM Cell and Quasi-Folded Data-Line Architecture", November 11, 1991, IEEE, Journal of Solid-State Circuit, pps. 1511-1518.
W		Takashima et al., "Open/Folded Bit-Line Arrangement for Ultra High-Density DRAMs", (Abstract), pps. 89-90.
W		Hidaka et al., "A Divided/Shared Bit-Line Sensing Scheme for ULSI DRAM Cores", Journal of Solid-State Circuit, Vol. 26, No. 4, April 1991, pps. 473-477.

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				Applicant Brent Keeth			
				Filing Date July 14, 2003		Group Art Unit 2818 Unknown	

U.S. PATENT DOCUMENTS						
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W	6,392,303	05/2002	Keeth			
W	6,429,529	08/2002	Keeth			
W	6,456,518	09/2002	Keeth			
W	6,504,255	01/2003	Keeth			
	6,594,173	07/2003	Keeth			

FOREIGN PATENT DOCUMENTS							
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO

OTHER DOCUMENTS		(Including Author, Title, Date, Pertinent Pages, Etc.)

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